MATHIC, SINGULAR & XMALLOC

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- **SINGULAR**
  - Signature-based Gröbner Basis algorithms
  - Restructuring SINGULAR
- **XMALLOC**
- **MATHIC**
  - Overall structure
  - Matrix reduction part
  - Methods of Parallelization
  - Future steps

Implementation of different variants of F5:

- Kernel implementation
  - Up to 10 times faster than SINGULAR's std implementation
  - Not using any linear algebra, plain polynomial reduction
  - Officially available in SINGULAR 4.0

Signature-based Gröbner Basis algorithms

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  - Officially available in SINGULAR 4.0
- Library implementation
  - together with John Perry
  - Teaching purpose only

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  - Gröbner layer
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First official release: End of 2013

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$\Longrightarrow$ XMALLOC

- standalone library with interface to SINGULAR
- step by step making it thread-safe
- keeping OMALLOC's speed and memory footprint when used in SINGULAR

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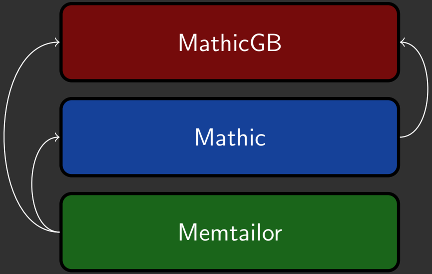
Main structure of the library

Consists of 3 big parts:



Gröbner basis structures and algorithms

Data types, structures, hashing

Small arena memory manager

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Note

The paper "Practical Groebner Basis Computation" by Roune and Stillman describes the data structures from a high level. The paper was presented at ISSAC12 and is available (in an extended version) at `http://arxiv.org/abs/1206.6940`.

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- End of 2012: A first working, parallel F4 implementation.

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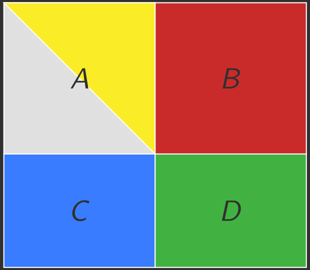

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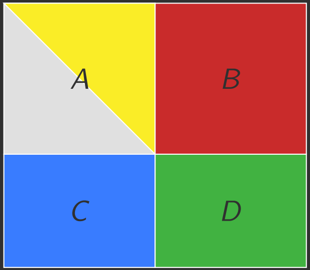

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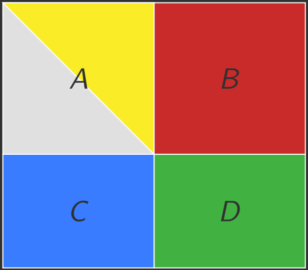
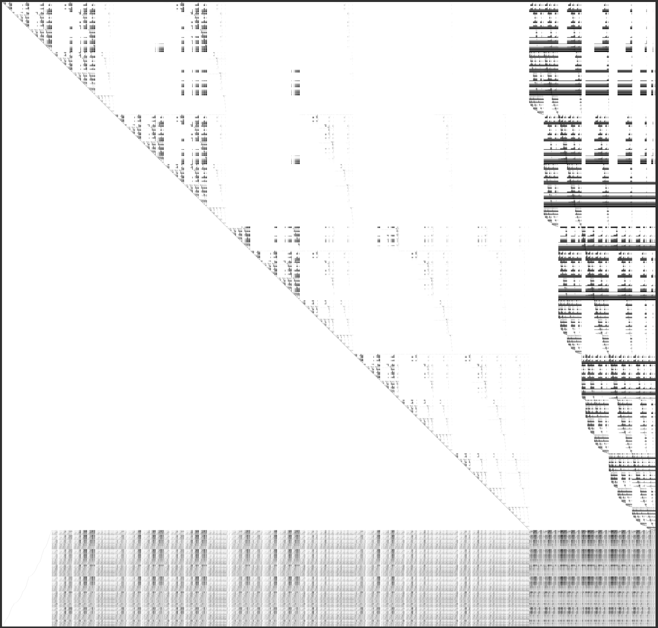


- Not reducing A, but directly eliminating C.
- Focussing on fields of prime characteristic $< 2^{16}$.
$\Rightarrow$ Delayed modulus when reducing D to D' by the surrounding parts.

How our matrices look like



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- Ongoing tasks: Matrix format, (parallel) matrix construction

Methods of Parallelization

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  - Until now only basic PARALLEL_FOR / BLOCKED_RANGE implementations.
  - Needs more abstraction on the task level.

Near future

- Do not double memory while preparing matrix
  Permuting rows and columns currently copies.
- Break matrices into smaller stripes of columns
  Enabling 16-bit column indices for each stripe; trying to put several rows of such a stripe into L1-cache.
- Finer graining in parallelization
  Until now only Intel Threading Blocks is used.

On the longer run

- Rewrite of the matrix reduction
  Right now it is a rather straightforward implementation; needs to become an own layer.
- F5F4
  Until now this is a plain F4 implementation. Signature-based computations are only available without linear algebra at the moment.
- Syzygy computations
- Investigating GPUs
  Whole new business when it comes to efficient implementation due to different architecture.

GIT repositories available

LELA

https://github.com/martani/LELA

SINGULAR

https://github.com/Singular/Sources

XMALLOC

https://github.com/ederc/xmalloc

MATHIC

https://github.com/broune/memtailor

https://github.com/broune/mathic

https://github.com/broune/mathicgb